U.S. Department of Commerce, Patent and Trademark	Atty. Docket No.	Application No.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	BTAT.002US1	09/832,933
	Applicant(s)	Conf. No.
(Use several sheets if necessary)	Wu et al.	5253
(Form PTO-1449)	Filing Date	Art Group
	April 11, 2001	2123

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
THS	1	6,498,515	12/24/02	Kawakami et al.			
V	2	6,414,498	7/2/02	Chen			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

THS	3	Hu, "Simulating Hot-Carrier Effects on Circuit Performance," *Semicond. Sci. Technol.* 7 (1992) B555-B558.
	4	Wu et al., "Full-Chip Reliability Simulation for VDSM Integrated Circuits," *Microelectronics Reliability* 41 (2001) pp. 1273-1278.
V	5	Seo et al., "The Hot Carrier Degradation and Device Characteristics with Variation of Pre-Metal Dielectric Materials," *Mat. Res. Soc. Symp. Proc.*, Vol. 544, 1999, pp. 179-184.

Examiner [signature]	Date Considered 10/19/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.

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U.S. Patent Documents

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THS	1	6,530,064	3/4/03	Vasanth et al.			
	2	5,615,377	3/25/77	Shimizu et al.			
	3	6,795,802	9/21/04	Yonezawa et al.			

U.S. Published Patent Application Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
THS	4	2003/0158713A1	8/21/03	Akimoto et al.			

Foreign Patent Documents

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		Document	Date	Country	Class	Subclass	Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

THS	5	Li et al., "A Probabilistic Timing Approach to Hot-Carrier Effect Estimation," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 13, No. 10, October 1994, pp. 1223-1234.
	6	IsSpice4 User's Guide, *Intusoft*, 1988-1996, pp. 196-216.
	7	Kawakami et al., "Gate-Level Aged Timing Simulation Methodology for Hot-Carrier Reliability Assurance," Proceedings of the ASP-DAC 2000, Asia and South Pacific, Jan. 25-28, 2000, pp. 289-294.
	8	Ye et al., "Developing Aged SPICE Model for Hot Carrier Reliability Simulation," Integrated Reliability Workshop Final Report, 2000, IEEE International, Oct. 23-26, 2000, pp. 153-154.

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